In the Claims

1-21. (Cancelled)

21. (New) Communication circuitry comprising:

a processing circuitry configured to receive a communication from a communication link;

a plurality of crossbar integrated circuits; and

a plurality of parallel channels between the processing circuitry and each crossbar integrated circuit of the plurality of crossbar integrated circuits, with the plurality of parallel channels of a particular crossbar integrated circuit being configured to transfer the communication and a clock signal in parallel to the particular crossbar integrated circuit.

22. (New) The communication circuitry of claim 21 wherein the plurality of parallel channels is comprised of parallel differential signal pairs and wherein one of the differential signal pairs is for the clock signal.

23. (New) The communication circuitry of claim 21 wherein the communication link comprises a serial channel.

24. (New) The communication circuitry of claim 21 wherein the communication comprises a data packet.

25. (New) The communication circuitry of claim 21 wherein the communication comprises a fixed-length data packet.

26. (New) The communication circuitry of claim 21 wherein the communication circuitry comprises a switch fabric.

27. (New) The communication circuitry of claim 21 wherein the processing circuitry is comprised of at least one virtual output queue that stores the communication prior to switching and that is associated with an egress port.

28. (New) The communication circuitry of claim 21 wherein the processing circuitry is comprised of at least one virtual output queue that stores the communication prior to switching and wherein a virtual output queue is comprised of sub-queues that are each associated with a particular priority.

29. (New) The communication circuitry of claim 21 wherein the processing circuitry is comprised of a multi-cast virtual output queue that stores the communication prior to switching for multi-cast output.

30. (New) The communication circuitry of claim 21 wherein the plurality of parallel channels include multiplexers to perform bit slicing through the crossbar integrated circuits.

31. (New) A method of operating communication circuitry, the method comprising:

receiving a communication in a processing circuitry from a communication link;

transferring the communication and a clock signal in parallel over a plurality of parallel channels to a particular crossbar integrated circuit of a plurality of crossbar integrated circuits; and

switching the communication in the particular crossbar integrated circuit based on the clock signal.

32. (New) The method of claim 31 wherein transferring the communication and the clock signal in parallel over the plurality of parallel channels comprises transferring the communication and the clock signal over parallel differential signal pairs.

33. (New) The method of claim 31 wherein transferring the communication and the clock signal in parallel over the plurality of parallel channels comprises transferring the communication and the clock signal over parallel differential signal pairs wherein one of the differential signal pairs is for the clock signal.

34. (New) The method of claim 31 wherein the communication comprises a data packet.

35. (New) The method of claim 31 wherein the communication comprises a fixed-length data packet.

36. (New) The method of claim 31 wherein the communication circuitry comprises a switch fabric.

37. (New) The method of claim 31 further comprising, in the processing circuitry, storing the communication in a virtual output queue that is associated with an egress port prior to switching.

38. (New) The method of claim 31 further comprising, in the processing circuitry, storing the communication in a virtual output sub-queue that is associated with a particular priority.

39. (New) The method of claim 31 further comprising, in the processing circuitry, storing the communication in a multicast virtual output queue that stores the communication prior to switching for multi-cast output.

40. (New) The method of claim 31 wherein transferring the communication and the clock signal in parallel comprises multiplexing the communications to perform bit slicing through the crossbar integrated circuits.